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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,694	05/16/2001	Yong-In Park	8733.428.00	9209
30827	7590	12/30/2003	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006			MALDONADO, JULIO J	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 12/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.



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09/555,694

05/16/2001

Yong-In Park

8733.428.00

EXAMINER

Maldonado, Julio J.

ART UNIT

PAPER

2893

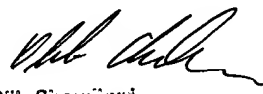
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Commissioner for Patents

The IDS filed 5/8/03 is attached.

  
Julie Chen  
Supervisory Patent Examiner  
Technology Center 2800

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Substitution for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	09/855,694
				Filing Date	May 16, 2001
				First Named Inventor	Yong-In Park
				Art Unit	2823
				Examiner Name	J. Maldonado
Sheet	1	of	1	Attorney Docket Number	8733.428.00-US

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
JUL	AA	4,604,294-	08-05-1986	Tanaka et al.	column 5, lines 4-9

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)			
JUL	BA	-61-256671-	11-14-1986	Matsumoto et al.	Abstract

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See attached Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the application number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature	Julio J. Maldonado	Date Considered	12/31/2003
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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Paper No. 20031223

Application Number: 09/855,694  
Filing Date: May 16, 2001  
Appellant(s): PARK ET AL.

**MAILED**

DEC 30 2003

**GROUP 2800**

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Yong-In Park  
Woong-Kwong Kim  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 10/03/2003.

**(1) *Real Party in Interest***

A statement identifying the real party in interest is contained in the brief.

**(2) *Related Appeals and Interferences***

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

**(3) *Status of Claims***

The statement of the status of the claims contained in the brief is correct.

**(4) *Status of Amendments After Final***

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) *Summary of Invention***

The summary of invention contained in the brief is correct.

**(6) *Issues***

The appellant's statement of the issues in the brief is correct.

**(7) *Grouping of Claims***

Appellant's brief includes a statement that claims 1-5, claims 6-8, claims 9-14, claims 15-17 and claims 18-20 stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

**(8) *Claims Appealed***

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(9) Prior Art of Record**

6,261,881

Yamazaki et al.

07-2001

**(10) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-5 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicants' admitted prior art in the instant application in view of Yamazaki et al. (U.S. 6,261,881).

In reference to claims 1, 5, 15 and 18, the prior art (Figs.1-4) in a method to form thin film transistors teaches forming a gate electrode (30) on a first substrate (1); forming an organic layer (33) over the first substrate (1) having the gate electrode (30); curing the organic layer (33) in a first chamber; transferring the first substrate (1) having the organic layer (33) from the first chamber to a second chamber; forming an active layer (34) on the organic layer (33) in the second chamber; forming source (38) and drain (40) electrodes on the active layer (34); forming a pixel electrode (14) connected to the drain electrode (40); and forming a liquid crystal layer (10) between the first substrate (1) and a second substrate (4) (page 2, line 11 – page 7, line 22).

The prior art fails to teach transferring the first substrate having the organic layer from a first chamber to a second chamber without exposing the first substrate having the organic layer to oxygen atmosphere during transfer. However, Yamazaki et al. (Figs.5, 13 and 14) in a related method to form thin film transistors teach transferring a first substrate (500) having an organic layer (503) from a first chamber (44) to a second chamber (45) without exposing the first substrate (500) having the organic layer (503) to oxygen atmosphere during transfer (column 9, line 23 – column 10, line 61 and column 15, line 4 – column 16, line 34). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention was made to deposit the organic layer over the first substrate and transfer it from one chamber to another without exposing the organic layer to the atmosphere as taught by Yamazaki et al. in the TFT process of the prior art, since this would improve the interface between an active layer and an insulating film (column 2, lines 40-49).

In reference to claims 2-4, 16, 17, 19 and 20, the prior art teaches the organic insulating layer (33) is selected from a group consisting of benzocyclobutene (BCB); the heating is performed to cure the organic layer under an inert gas condition, said inert gas includes nitrogen gas (N<sub>2</sub>); and the active layer (34) includes an amorphous silicon layer and a doped amorphous silicon layer (page 2, line 11 – page 7, line 22).

**(11) Response to Argument**

Appellants' arguments filed 10/03/2003 have been fully considered but they are not persuasive.

Appellants argue that Yamazaki et al. "...is concerned with... the interface between the second gate insulating layer and the semiconductor layer described in embodiment 3, not the interface between the first gate insulting layer (BCB) and the second insulating layer (SiN<sub>x</sub> or SiO<sub>2</sub>). As such, Yamazaki et al. fails to teach 'curing the organic insulating layer' and 'forming a silicon layer on the organic insulating layer in the equipment without breaking the vacuum' as recited in the claim 1, and 'curing the organic layer in a first chamber' and forming an active layer on the organic layer in the second chamber', as recited in claims 15 and 18..."

In response to this argument, Yamazaki et al. teach a method of forming thin film transistor (TFT) devices, wherein in all the embodiments of the invention, forming on a semiconductor substrate having a gate wiring formed thereon, a gate insulating film, an initial semiconductor film and an insulating film without exposing them to air (column 5, lines 3 – 6, lines 23 – 26 and lines 46 – 49, for example). Furthermore, in the description of the apparatus used to form such layers (see Figs.13 and 14), Yamazaki et al. teach forming such layers in different chambers, and transferring the substrate from chamber to chamber without exposing it to air (column 9, lines 8 – 22). This air-devoid atmosphere is achieved by first by establishing a high vacuum state in all the chambers used, followed by purging with nitrogen (column 9, lines 39 – 42). Having this in mind, Yamazaki et al. was recited to teach a process in which a TFT device was formed in a vacuum to avoid the presence of oxygen to improve the interface between layers (column 9, lines 8 – 42). Specifically, in the third embodiment of the invention (Fig.5), Yamazaki et al. teach using benzocyclobutene (BCB) as an insulating layer for



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the purpose of achieving a planar surface (column 15, lines 4 – 43). In other words, the object of citing Yamazaki et al. was that the reference specifically teaches transporting the substrate from one stage to another in a highly vacuum state to prevent contamination of the surface of the substrate. And the combination of the teachings of Yamazaki et al. in the prior art would arrive to the claimed invention, i.e., “forming a silicon layer on the organic layer without breaking the vacuum as recited in claim 1; and transferring the organic layer from a first chamber to a second chamber and forming an active layer on the organic layer in the second chamber without exposing the substrate having the organic layer to oxygen atmosphere during transfer in claims 15 and 18” as argued. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

For the above reasons, it is believed that the rejections should be sustained.

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Art Unit: 2823

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Respectfully submitted,

Julio J. Maldonado  
Examiner  
Art Unit 2823



JMR  
December 23, 2003

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